REMARKS

I. STATUS OF THE CLAIMS:

Claims 1, 11, 20 and 29 have been amended. Support for the amendments can be found in FIG. 1.

New claim 36 has been added and is somewhat similar to claim 1.

Claims 1-36 are pending and under consideration. Reconsideration is respectfully requested.

II. OBJECTION TO THE ABSTRACT:

The Abstract has been amended. Therefore, it is respectfully submitted that the objection is overcome.

III. OBJECTION TO THE SPECIFICATION:

The Specification has been amended in accordance with the Examiner's comments at page 3 of the Office Action. Therefore, it is respectfully submitted that the objection is overcome.

IV. REJECTION OF CLAIMS 11-12 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH:

Claim 11 has been amended to overcome this rejection. Based on the amendments to claim 11, the rejection of claim 12 is overcome.

V. REJECTION OF CLAIMS 1-3, 6-22, 25-35 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER TAGUCHI ET AL. (US PATENT NO. 5,915,025; HEREINAFTER "TAGUCHI"), AND FURTHER IN VIEW OF CURRAN ET AL. (US PATENT NO. 4,525,599; HEREINAFTER "CURRAN"):

The present invention as recited in claim 1, for example, relates to a processing apparatus. The processing apparatus comprises an internal circuit including a CPU executing programs, at least one internal device having a predetermined function and a bus line connecting said CPU to said internal device, extending externally and transferring an address and data, wherein said internal circuit includes at least one internal memory as an internal device. The processing apparatus further comprises an external circuit provided externally of an

externally extending portion of said bus line and including at least one external device having a predetermined function, wherein said external circuit includes at least one external memory as an external device. The internal circuit also includes a ciphering section interposed at an entrance to an external side and ciphering the address and the data on the bus line by ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device.

Taguchi discloses a data processing apparatus with software protecting functions and a method including generating an encryption key depending on an attribute of data to be encrypted, generating a decryption key depending on an attribute of encrypted data, encrypting data to be encrypted by use of the encryption key, storing the encrypted data, decrypting the encrypted data by use of the decryption key, and outputting processed data to be encrypted (see column 4, lines 1-14). Further, Taguchi discloses at FIG. 31, a data processing apparatus comprising a data processing means, distributing software decryption means, encryption means, decryption means, key supply means, algorithm supply means and encryption method selection means all housed within a protective enclosure.

However, Taguchi fails to disclose "an external circuit". Further, element 150 shown in FIG. 31 of Taguchi which the Examiner considers to be an internal circuit, does not include "an internal memory" as in the claimed invention.

At page 5 of the Office Action, the Examiner admits that Taguchi fails to disclose "ciphering of the address" as recited in claim 1. However, the Examiner asserts that Curran discloses software which can be protected from illegal copying by encrypting the addresses of the data being accessed".

The Applicants respectfully submit that Curran discloses a method of encrypting program information stored in a memory and implementing encryption/decryption circuitry interposed between the memory and the central processor of a computer (see column 1, lines 50-56).

However, neither Taguchi nor Curran, individually or combined, disclose "said internal circuit includes at least one internal memory as an internal device [and] ...said external circuit includes at least one external memory as an external device," as recited in amended claim 1. Therefore, the combination of Taguchi and Curran fails to disclose the advantage of preventing illicit accesses to an internal memory via an add-on external device as in the claimed invention.

Accordingly, the combination of Taguchi and Curran fails to establish a prima facie case of obviousness over the claimed invention.

Although the above comments are specifically directed to claim 1, it is respectfully submitted that the comments would be helpful in understanding differences of various other rejected claims over the cited reference. Therefore, it is respectfully submitted that the rejection is overcome.

VI. REJECTION OF CLAIMS 4 AND 23 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER TAGUCHI IN VIEW OF CURRAN AND FURTHER IN VIEW OF IBM (IBM TECHNICAL DISCLOSURE BULLETIN 19800601):

As mentioned above, neither Taguchi nor Curran, individually or combined, disclose all of the features recited in claims 1 and 20 from which claims 4 and 23 respectively depend.

At page 9 of the Office Action, the Examiner admits that the combination of Taguchi and Curran fails to disclose any information regarding "timing at which said external circuit is not accessed". However, the Examiner asserts that IBM makes up for this deficiency.

Although IBM discloses testing memory devices by generating random addresses, IBM fails to make up for the deficiencies of Taguchi and Curran as mentioned above. Therefore, it is respectfully submitted that the rejection is overcome.

VII. REJECTION OF CLAIMS 5 AND 24 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER TAGUCHI IN VIEW OF CURRAN AND FURTHER IN VIEW OF MILHAUPT ET AL. (US PATENT NO. 5,706,445; HEREINAFTER "MILHAUPT"):

The Examiner admits that neither Taguchi nor Curran, disclose "using separate clocks with the encryption clock being set at a higher frequency that the processor clock". However, the Examiner asserts that Milhaupt makes up for the deficiencies of the combination of Taguchi and Curran.

Milhaupt discloses a data source supplying data and successive control signal indicative of valid-data, wherein transitions occur in the data during intervals between the signal indicative of valid-data, and a selector having a first input connected to the data source, and a second input, and an output. A circuit is connected to the output of the selector to receive data from the data source via the selector. A source of a quieting signal is connected to the second input, and the selector is responsive to the control signals to select the quieting signal during at least a portion of the interval between the signals indicative of valid-data, and to select the data source in response to at least some of the control signal indicative of valid-data (see column 2, lines 15-30).

However, neither of the foregoing references relied upon, individually or combined, disclose all of the features recited in claims 1 and 20 from which claims 5 and 24 respectively

depend. Therefore, it is respectfully submitted that the rejection is overcome.

VIII. INFORMATION DISCLOSURE STATEMENT:

In the IDS attached to the Office Action, the Examiner did not acknowledge references AG, AH and AL on the IDS filed January 31, 2003. However, these references were cited on a European Search Report filed with the IDS. The Applicants respectfully request that these references be acknowledged.

IX. CONCLUSION:

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: November 15, 2004

By: Deidre M. Davis

Deidre M. Davis
Registration No. 52,797

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501